DETAILED ACTION

REMARKS

1. Applicants' appeal brief filed April 3, 2008 responding to the November 15, 2007 Office Action provided in the rejection of claims 1-20, wherein no claims have been amended and no new claims have been added. Claims 1-20 remain pending in the application and which have been fully considered by the examiner.

2. The Examiner withdraws the non-statutory obviousness double patenting rejection of claim 1 over claims 1, 4, and 5 of copending application 10/969,789 and claims 11, 15, and 16 over claim 24 of copending application 10/735,934 corresponding to Applicants' filing of two terminal disclaimer.

3. The terminal disclaimer filed on **March 12, 2008** disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of **10/735,934** has been reviewed and is accepted. The terminal disclaimer has been recorded.

4. The terminal disclaimer filed on **March 12, 2008** disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of **10/969,789** has been reviewed and is accepted. The terminal disclaimer has been recorded.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an email from attorney of record, Kermit D. Lopez, dated May 23, 2008.

The application has been amended as follows:

IN THE SPECIFICATION:

1. Page 15 line 15 added the following brief description of Fig. 21:

   Fig. 21 illustrates a portion of an adaptive integration network with two loops.

2. Page 24 paragraph [0096] changed to:

   Nanoconnections 572, 574, 576, 578, and 580 may comprise nanoconductors such as, for example, nanotubes and/or nanowires. Nanoconnections 572, 574, 576, 578, and 580 thus comprise one or more nanoconductors. Additionally, input lines 522, 524, 526, 528, and 530 are respectively coupled to a plurality of input lines 542, 544, 546, 548 and 550, which are in turn each respectively coupled to nanoconnections 582, 584, 586, 588, and 590.

3. Page 28 paragraph [00108] changed to:

The physical neural network disclosed herein thus has a number of broad applications. The core concept of a Knowm^{TM} physical neural network, however, is basic. The very basic idea that the connection values between electrode junctions by nanoconductors can be used in a neural network device is all that required to develop an enormous number of possible configurations and applications thereof.

4. Page 44 paragraph [00160] changed to:

Note that connection network 1328 is labeled C2 in FIG. 13. A first signal can be output from connection network 1328 at node 1331. Likewise, a second signal can be output from connection network 1328 at node 1333. A resistor 1330, which is labeled R_b, is coupled between node 1331 and ground 1309. Also, a resistor 1334, which is also labeled R_b, is connected between node 1333 and ground 1309. Node 1333 is further connected to an input 1353 to amplifier 1338, while node 1331 is further coupled to an input 1351 to amplifier 1336. Note that resistor 1330 is also coupled to input 1351 at node 1331, while resistor 1334 is connected to input 1353 at node 1333.

5. Page 44 paragraph [00161] changed to:

A voltage V_1 can be measured at an input 1335 to amplifier 1336 and an input 1337 to amplifier 1338. Amplifiers 1336 and 1338 can be respectively referred to as neurons C and D. An output from amplifier 1336 is connected to a NOT gate 1340, which provides a signal that is input to a NOR gate 1342. Additionally, amplifier 1338 provides a signal,

which can be input to NOR gate 1342. Such a signal, which is output from amplifier 1338 can form an inhibitory signal, which is input to NOR gate 1342. Similarly, the output from amplifier 1336 can comprise an excitatory signal, which is generally input to NOT gate 1340. The excitatory and inhibitory signals respectively output from amplifiers 1336 and 1338 form an excitatory/inhibitory signal pair. NOR gate 1342 generates an output, which is input to an amplifier 1344 at input node 1347. A voltage V_d can be measured at input node 1346, which is coupled to amplifier 1344.

IN THE CLAIMS:

Claim 1

A system, comprising:

a physical neural network configured utilizing nanotechnology and integrated with feedback circuitry, wherein said physical neural network comprises a plurality of nanoconductors comprising at least one of nanotubes, nanowires, or nanoparticles, suspended and free to move about in a dielectric medium and which form neural connections between pre-synaptic and post-synaptic components of said physical neural network; and

a learning mechanism for applying Hebbian learning to said physical neural network.

Claims 8-10 (cancelled).

Claim 11

A system, comprising:

a physical neural network configured utilizing nanotechnology and integrated with feedback circuitry, wherein said physical neural network comprises a plurality of nanoconductors comprising at least one of nanotubes, nanowires, or nanoparticles, suspended and free to move about in a dielectric medium and which form neural connections between pre-synaptic and post-synaptic components of said physical neural network; and

a learning mechanism for applying Hebbian learning to said physical neural network wherein said learning mechanism utilizes a voltage gradient or pre-synaptic and post-synaptic frequencies thereof to implement Hebbian or anti-Hebbian plasticity within said physical neural network.

Claims 12-14 (cancelled).

Claims 17-20 (cancelled).

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

Claims 1-7, 11, and 15-16 are considered allowable since when reading the claims in light of the specification, as per MPEP §2111.01, none of the references of record alone

or in combination disclose or suggest the combination of limitations specified in independent claims 1, 11, and 17 including a physical neural network configured utilizing nanotechnology (supported at e.g., paragraphs [0087] to [0092]), wherein said physical neural network comprises a plurality of nanoconductors (supported at e.g. paragraph [0020]) suspended and free to move about in a dielectric medium (supported at e.g. paragraphs [0087] to [0092]), integrated with feedback circuitry (supported at e.g., paragraph [00117], a learning mechanism for applying Hebbian learning (supported at e.g., paragraphs [0028] to [0029]).

The closest prior art Jackson et al (U. S. Patent No. 6,536,106) discloses a process of manufacturing including a technique of assembling parts of an apparatus, wherein this technique forms electrode structures on a substrate, suspending the apparatus parts in a dielectric medium between electrodes of the electrode structure and using near-field electric field forces to align the parts in a predetermined position.

However, Jackson fails not teach a physical neural network integrated with feedback circuitry.

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai T. Tran whose telephone number is (571)272-4238. The examiner can normally be reached on 10:00 am - 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David R. Vincent can be reached on (571) 272-3080. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/mtt/
Examiner, Art Unit 2129

/David R Vincent/

Supervisory Patent Examiner, Art Unit 2129